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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,412	04/09/2004	Anders Landin	5681-01601	8427

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EXAMINER	
ELAND, SHAWN	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/22/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,412	LANDIN ET AL.	
	Examiner	Art Unit	
	Shawn Eland	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004, 27 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/11/05 & 09/12/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Liencres (US 5,434,993).

In regards to claim 1, Liencres teaches a node including an active device ***(see element 21)***, a memory ***(see element 37)***, and an interface coupled by an address network and a data network ***(see element 31)***; an additional node coupled to send a coherency message to the interface in the node via an inter-node network, wherein the coherency message requests an access right to a coherency unit ***(see figure 3a; see column 6, lines 11 – 15)***; wherein in response to the coherency message, the interface is configured to send a first type of address packet on the address network if a global access state of the coherency unit in the node is a modified state and to send a second type of address packet if the global access state is not the modified state ***(see column 8, lines 63 – 68 through column 9, lines 1 – 8)***; wherein in response to the second type of packet, the memory is configured to send a data packet corresponding to the coherency unit on the data network, regardless of whether the memory has an ownership responsibility for the coherency unit ***(see column 2, lines 22 – 30)***.

In regards to claim 13, Liencres teaches a plurality of devices including a memory ***(see element 37)***, an active device ***(see element 21)***, and an interface configured to send and receive coherency messages on an inter-node network coupling nodes in the multi-node system ***(see element 31)***; an address network configured to convey address packets between the plurality of devices ***(see element 33)***; a data network configured to convey data packets between the plurality of devices ***(see element 33)***; wherein in response to receiving a coherency message on the inter-node network requesting an access right to a coherency unit, the interface is configured to send a first type of address packet on the address network if a global access state of the coherency unit in the node is a modified state and to send a second type of address packet on the address network if the global access state of the coherency unit in the node is not the modified state ***(see column 8, lines 63 – 68 through column 9, lines 1 – 8)***; wherein the memory is configured to respond to receipt of the second type of address packet by sending a data packet corresponding to the coherency unit on the data network, regardless of whether the memory currently has an ownership responsibility for the coherency unit ***(see column 2, lines 22 – 30)***.

In regards to claim 24, Liencres teaches an interface in the node receiving a coherency message requesting an access right to a coherency unit via the inter-node network from an additional interface in the additional node ***(see element 33)***; the interface sending an address packet on an address network in the node in response to said receiving, wherein the address packet is a first type of address packet if the global access state of the coherency unit in the node is a modified state and a second type of

address packet if the global access state is not the modified state ***(see column 8, lines 63 – 68 through column 9, lines 1 – 8)***; in response to said sending, a memory in the node providing the interface with data corresponding to the coherency unit regardless of whether the memory has an ownership responsibility for the coherency unit if the address packet is the second type of address packet ***(see column 2, lines 22 – 30)***.

For claims 2, 14, & 25, Liencres teaches the coherency message requests a read access right to the coherency unit ***(see column 7, "Read Transactions")***, wherein the first type of address packet is a proxy read-to-share-modified packet ***(see figure 1d)*** and wherein the second type of address packet is a proxy memory read packet ***(see figure 1c)***.

For claim 3, Liencres teaches if the active device has the ownership responsibility for the coherency unit, the active device is configured to send a data packet corresponding to the coherency unit to the interface via the data network in response to receipt of the proxy read-to-share-modified packet ***(see column 7, "Read Transactions")***.

For claim 15, Liencres teaches if the active device is the owner of the coherency unit, the active device is configured to send data corresponding to the coherency unit to the interface in response to receipt of the proxy read-to-share-modified packet ***(see column 7, "Read Transactions")***.

For claim 26, Liencres teaches an active device included in the node sending data corresponding to the coherency unit to the interface in response to receipt of the

proxy read-to-share-modified packet if the active device has the ownership responsibility for the coherency unit ***(see column 7, "Read Transactions")***.

For claim 4, Liencres teaches if the active device has the ownership responsibility for the coherency unit, the active device is configured to lose its ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet ***(see column 9, lines 22 – 31)***.

For claim 16, Liencres teaches if the active device is the owner of the coherency unit, the active device is configured to lose its ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet ***(see column 9, lines 22 – 31)***.

For claim 27, Liencres teaches the active device losing the ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet if the active device has the ownership responsibility for the coherency unit ***(see column 9, lines 22 – 31)***.

For claim 5, Liencres teaches if the active device has the ownership responsibility for the coherency unit, the active device is configured to transition an access right to the coherency unit upon sending the data packet on the data network ***(see column 7, "Read Transactions")***.

For claims 6 & 22, Liencres teaches the address network is configured to convey the first and second types of address packet from the interface to a directory in point-to-point mode ***(see element 33 in figure 3a; having only 2 processors would, in effect, be a point-to-point mode)***.

For claim 28, Liencres teaches the address network conveying the first and second types of address packet from the interface to a directory in point-to-point mode ***(see element 33 in figure 3a; having only 2 processors would, in effect, be a point-to-point mode)***.

For claim 7, Liencres teaches the address network is configured to convey the first and second types of address packet from the interface to a plurality of devices included in the node in broadcast mode, wherein the plurality of devices include the memory and the active device ***(see column 4, lines 45 – 49)***.

For claim 23, Liencres teaches the address network is configured to convey the first and second types of address packet from the interface to the plurality of devices in broadcast mode ***(see column 4, lines 45 – 49)***.

For claim 29, Liencres teaches the address network conveying the first and second types of address packet in broadcast mode ***(see column 4, lines 45 – 49)***.

For claims 8 & 21, Liencres teaches the data packet sent by the memory includes an indication of the global access state of the coherency unit in the node ***(see column 7, lines 48 – 52)***.

For claim 9, Liencres teaches the coherency message requests a shared access right to the coherency unit ***(see figure 1d)***.

For claim 10, Liencres teaches the additional node is configured to send the coherency message in response to an additional active device included within the additional node sending an address packet on an additional address network included within the additional node, wherein the address packet requests write access to the

coherency unit, wherein the coherency unit is in a shared global access state in the additional node, and wherein the node is a home node of the coherency unit ***(see column 8, lines 63 – 68)***.

For claim 30, Liencres teaches the additional node sending the coherency message in response to an additional active device included within the additional node sending an address packet on an additional address network included within the additional node, wherein the address packet requests write access to the coherency unit, wherein the coherency unit is in a shared global access state in the additional node, and wherein the node is a home node of the coherency unit ***(see column 8, lines 63 – 68)***.

For claims 11 & 31, Liencres teaches if the coherency unit is in the shared global access state in any of the plurality of nodes other than the home node, the coherency unit is in the shared global access state in the home node and no active device and no memory subsystem included in any of the plurality of nodes has the ownership responsibility for the coherency unit ***(see figure 1a; see column 2, lines 15 – 24)***.

For claim 12, Liencres teaches the interface is configured to send a copy of the coherency unit included in the data packet to the additional node ***(see column 7, "Read Transactions")***.

For claim 20, Liencres teaches the data packet sent by the memory includes a copy of the coherency unit ***(see column 7, "Read Transactions")***.

For claim 32, Liencres teaches the interface sending a copy of the coherency unit included in the data packet to the additional node ***(see column 7, "Read Transactions")***.

For claim 17, Liencres teaches the interface includes a global access state cache indicating global access states of a plurality of recently accessed coherency units in the node ***(see element 31)***.

For claim 18, Liencres teaches the interface is configured to check the global access state cache for the global access state of the coherency unit in the node, wherein if the global access state of the coherency unit is not included in the global access state cache, the interface is configured to request an indication of the global access state of the coherency unit from the memory ***(see column 9, lines 14 – 31)***.

For claim 19, Liencres teaches the interface is configured to request the global access state of the coherency unit in the node from the memory by sending the second type of address packet to the memory ***(see column 9, lines 14 – 31)***.

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
12/26/06

Examiner Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on Monday - Thursday from 7:30am to 5:00pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough, can be reached on (571) 272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SE

Shawn Eland
12/21/2006